

FIG. 1(A)

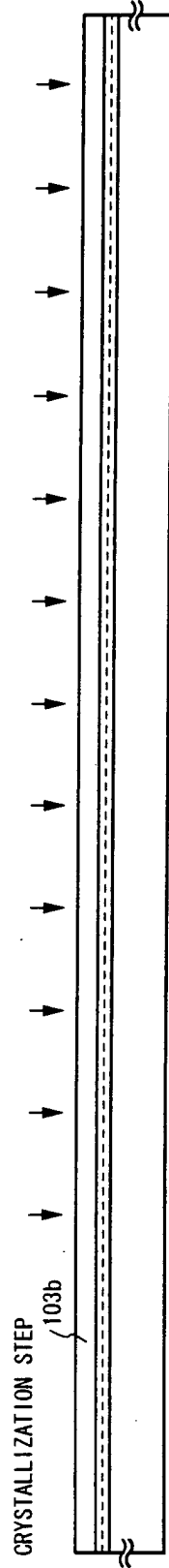


FIG. 1(B)

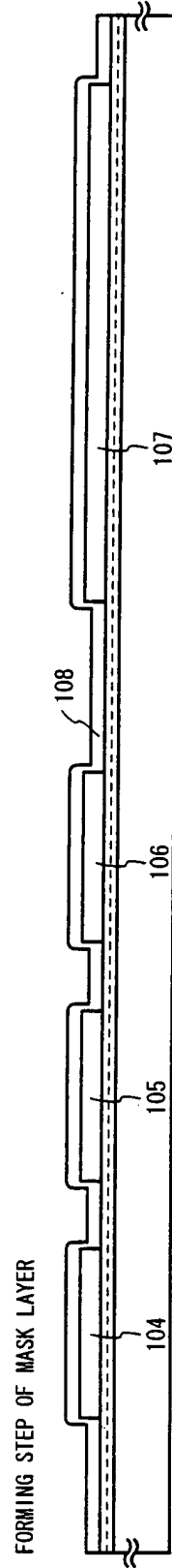


FIG. 1(C)

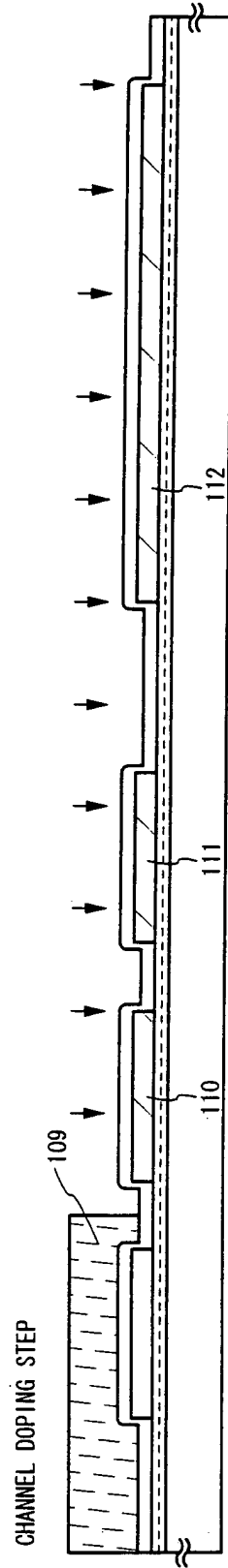


FIG. 1(D)

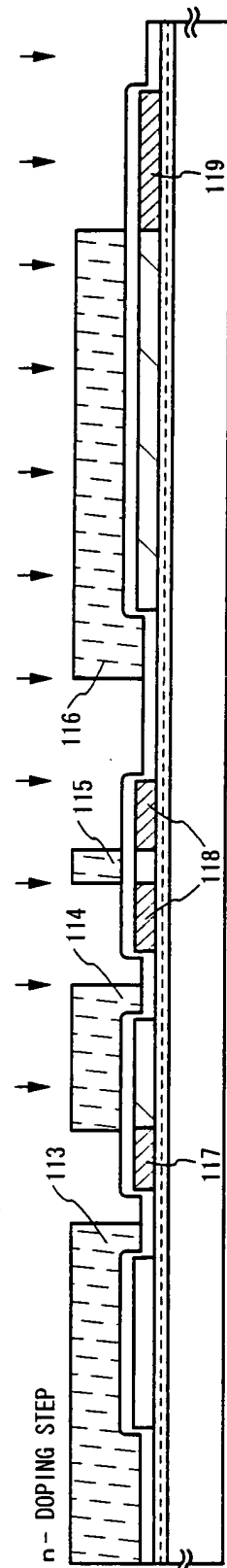


FIG. 2(A)

MASK LAYER REMOVING STEP/LASER ACTIVATING STEP/FORMING STEP OF GATE INSULATING FILM

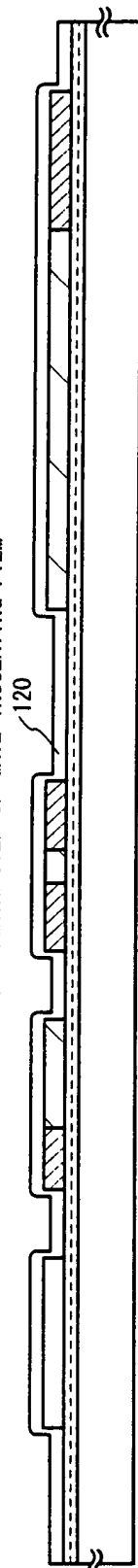


FIG. 2(B)

FORMING STEP OF FIRST CONDUCTIVE LAYER

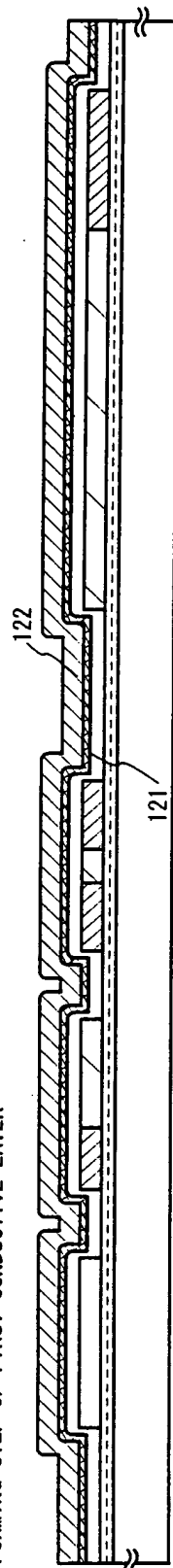


FIG. 2(C)

FORMING STEP OF GATE ELECTRODE

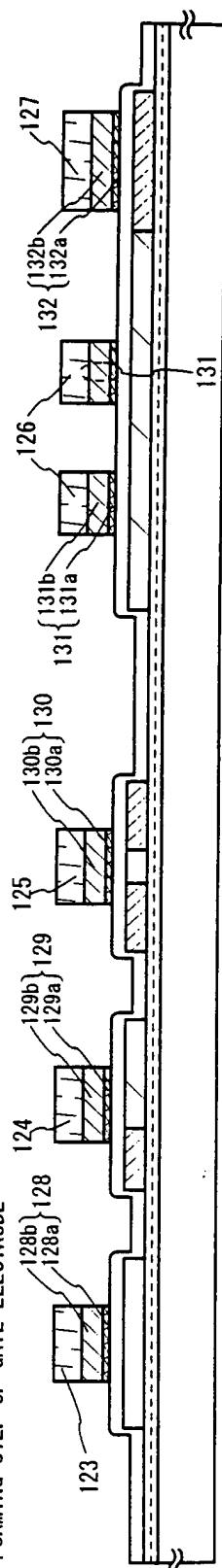


FIG. 2(D)

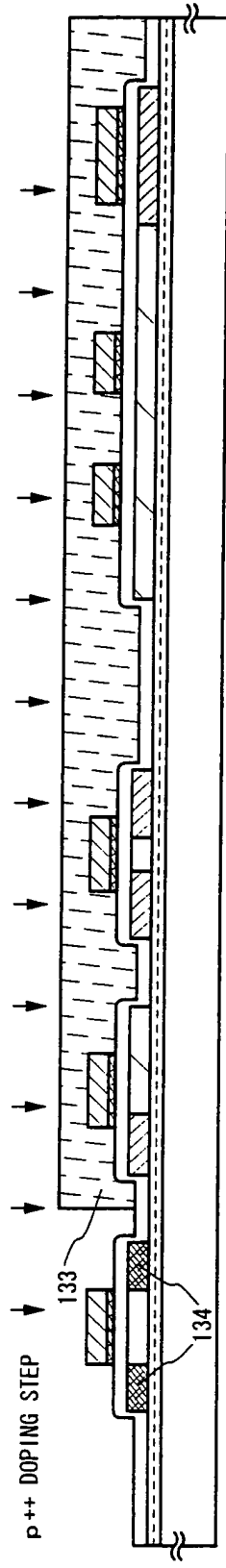


FIG. 3(A)

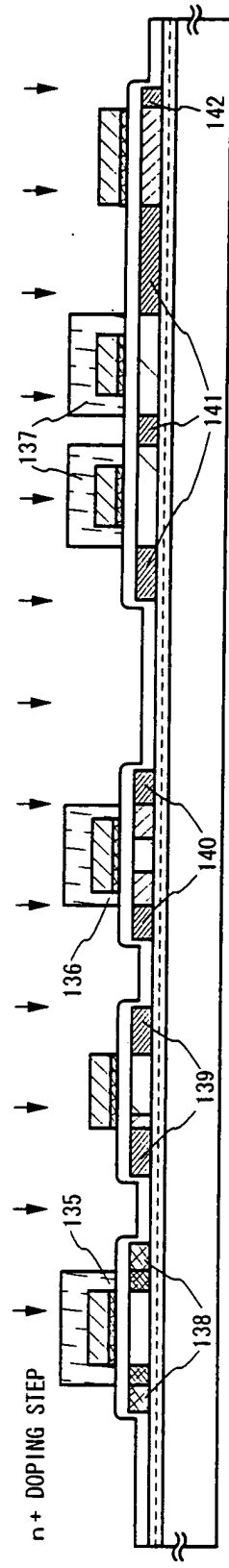


FIG. 3(B)

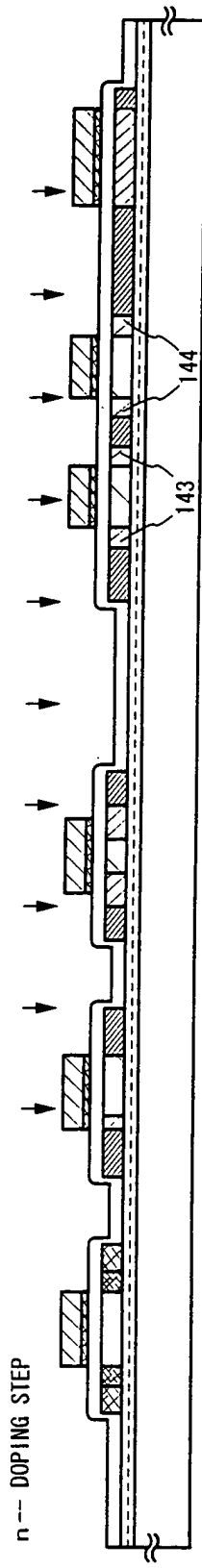


FIG. 3(C)

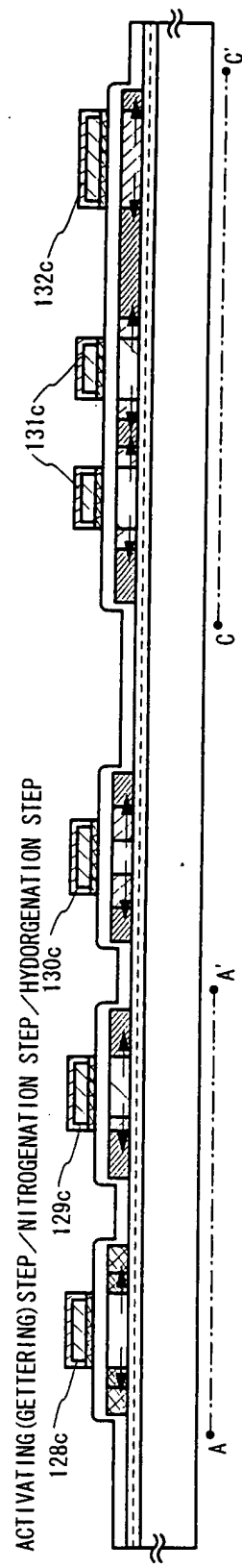


FIG. 3(D)

FORMING STEP OF SECOND CONDUCTIVE LAYER

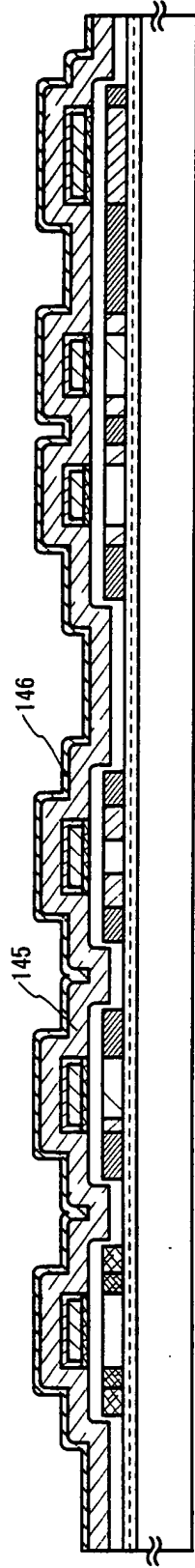


FIG. 4(A)

FORMING STEP OF GATE WIRING

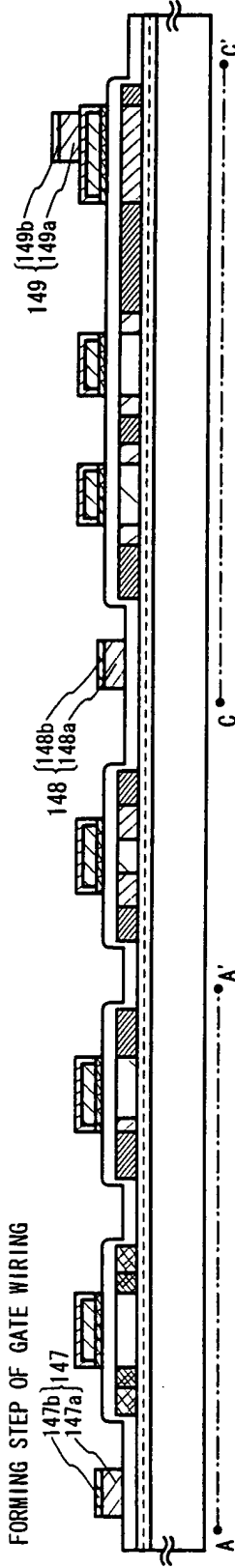


FIG. 4(B)

FORMING STEP OF INTERLAYER INSULATING FILM/FORMING STEP OF CONTACT HOLE/FORMING STEP OF WIRING/  
FORMING STEP OF PASSIVATION FILM

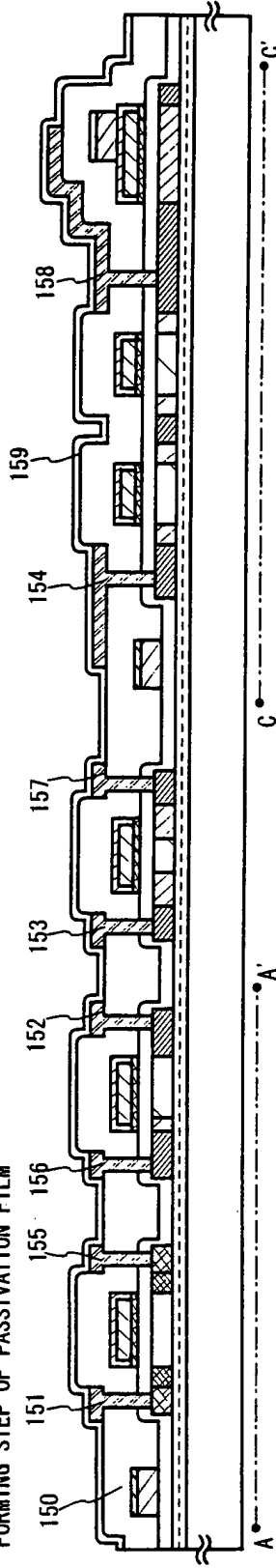


FIG. 4(C)

This cross-sectional view illustrates the layered structure of a pixel portion in a semiconductor device. The device is divided into three main functional regions from left to right: the CMOS circuit, the first N-channel TFT, and the second N-channel TFT. The CMOS circuit includes a P-channel TFT (201) and an N-channel TFT (202). The first N-channel TFT region contains a first N-channel TFT (203) and a second N-channel TFT (204). The second N-channel TFT region contains a storage capacitor (205). The structure is built on a substrate (101) with various layers including gate insulators (102, 103), gate electrodes (104, 105), and channel layers (106, 107). The pixel TFTs (203, 204) are connected to a common source line (108) and a common drain line (109). The storage capacitor (205) is connected to the common drain line (109) and a storage electrode (110). The pixel portion is connected to a data line (111) and a pixel electrode (112). The device is protected by a passivation layer (113) and a protective film (114).

Labels and components shown in the diagram include:

- CMOS CIRCUIT:** 201: P CHANNEL TFT, 202: FIRST N CHANNEL TFT, 203: SECOND N CHANNEL TFT.
- PIXEL TFT:** 204: PIXEL TFT.
- STORAGE CAPACITOR:** 205: STORAGE CAPACITOR.
- Pixel Portion:** 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114.
- Other Labels:** 150, 147, 151, 128, 155, 156, 129, 152, 104, 153, 157, 130, 154, 163, 159, 164, 131, 165, 149, 107, 161, 160, 162, 120, 224, 220, 218, 221, 225, 222, 219, 223, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300.

FIG. 5

FIG. 6(A)

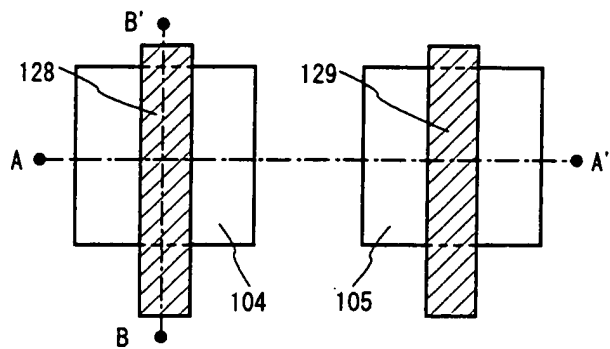


FIG. 6(B)

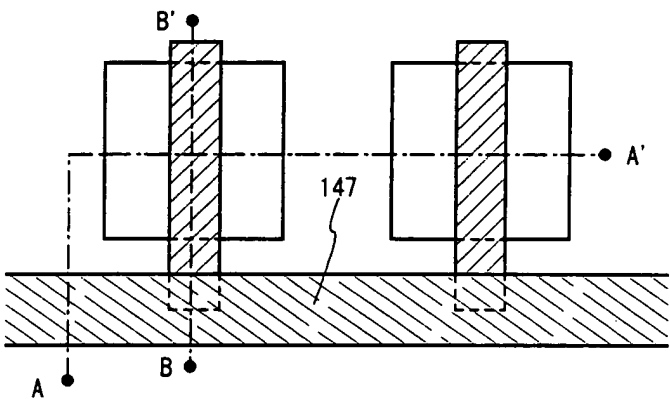


FIG. 6(C)

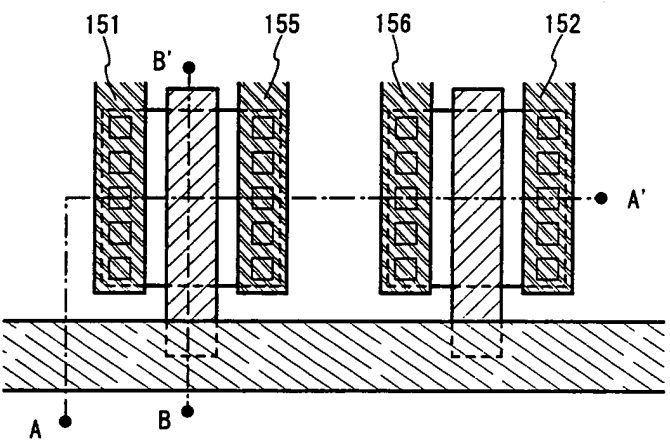


FIG. 7(A)

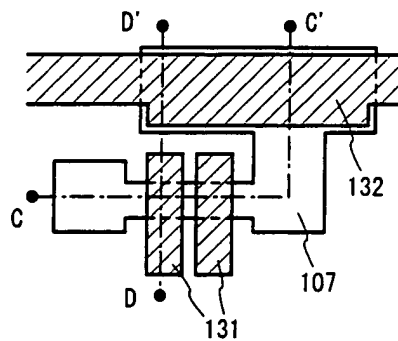


FIG. 7(B)

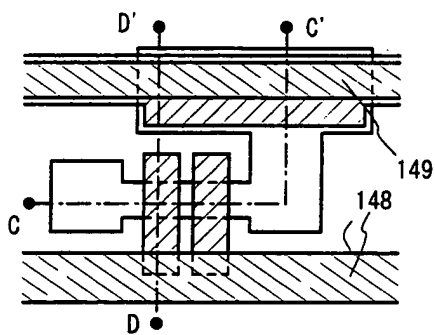


FIG. 7(C)

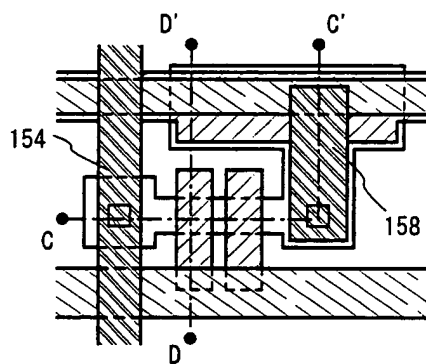


FIG. 8(A)

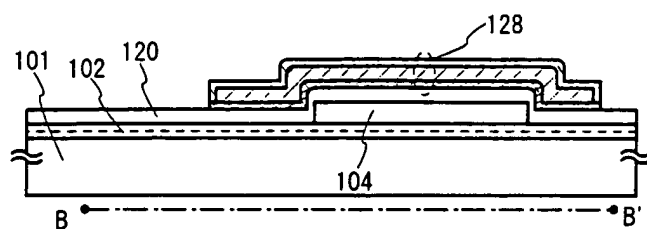


FIG. 8(B)

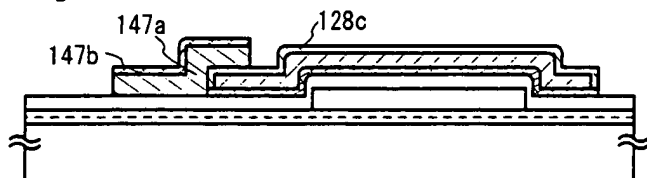


FIG. 8(C)

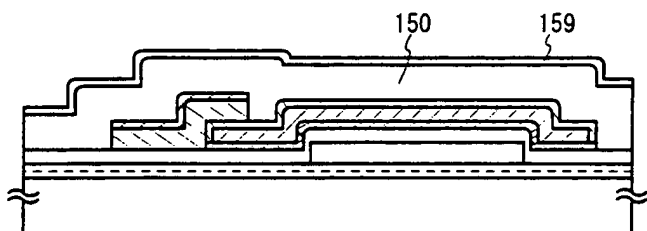


FIG. 9(A)

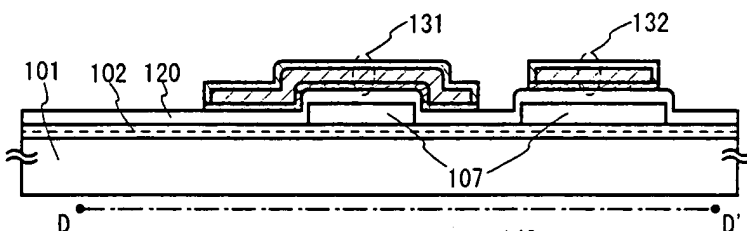


FIG. 9(B)

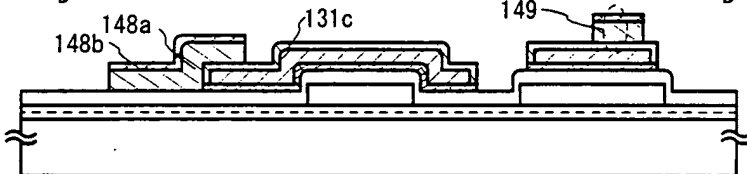
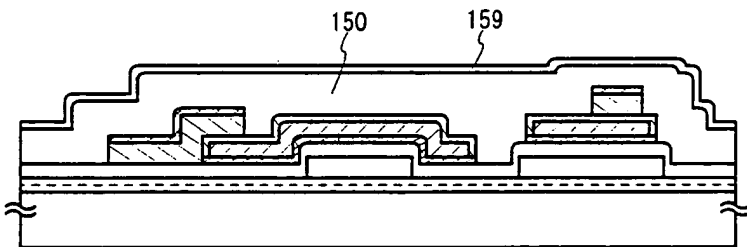


FIG. 9(C)





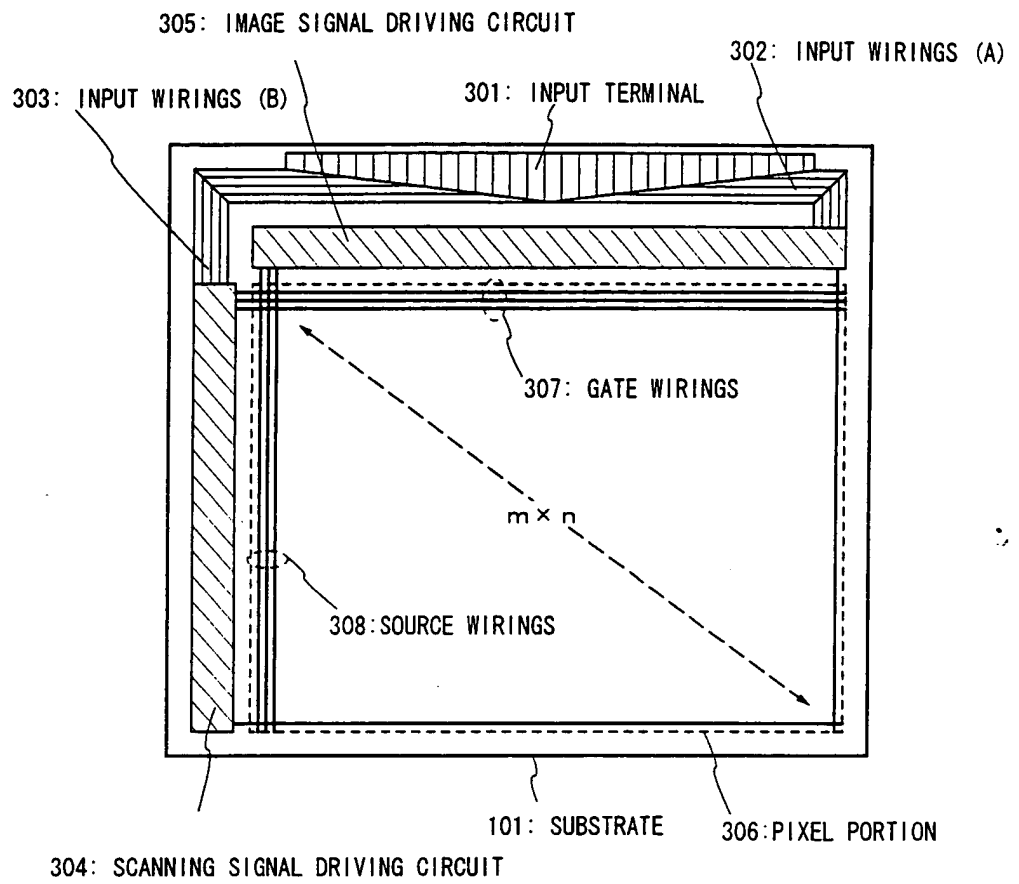


FIG. 10

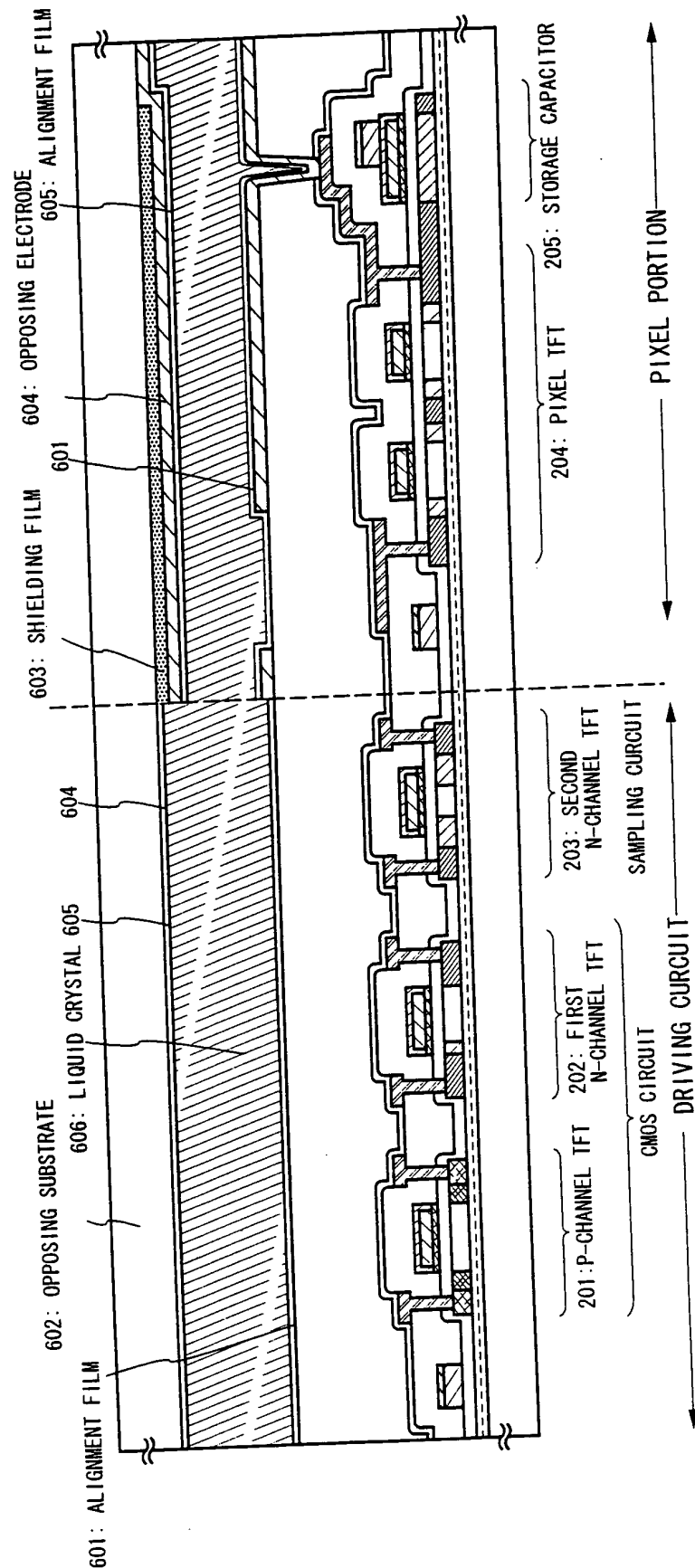


FIG. 11

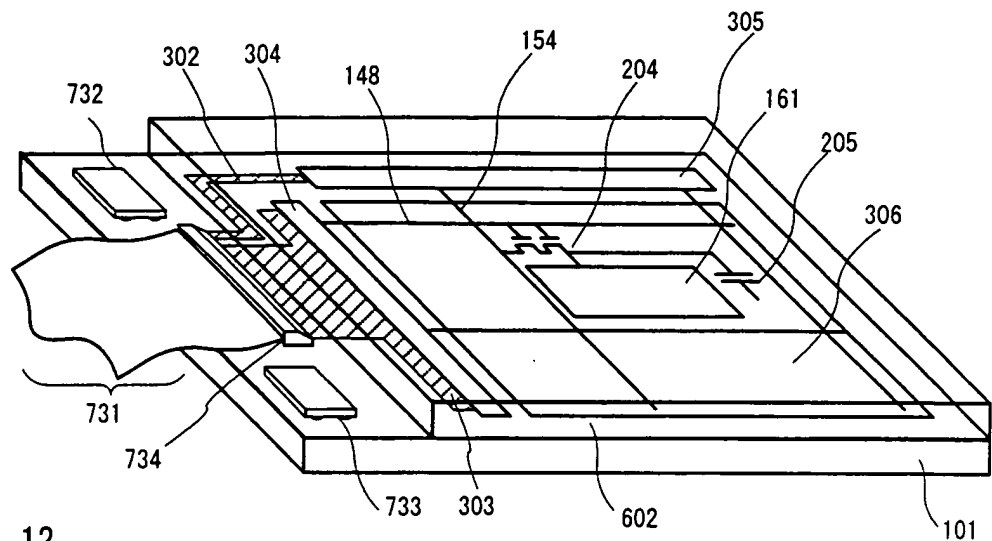


FIG. 12

101 : SUBSTRATE  
 306 : PIXEL PORTION  
 302, 303 : INPUT WIRINGS  
 304 : SCANNING SIGNAL DRIVING CIRCUIT  
 305 : IMAGE SIGNAL DRIVING CIRCUIT  
 731 : FPC  
 732, 733 : IC CHIP  
 734 : external I/O terminal  
 204 : PIXEL TFT  
 148 : GATE WIRINGS  
 154 : SOURCE WIRINGS  
 161 : PIXEL ELECTRODE  
 205 : STORAGE CAPACITOR  
 602 : OPPOSING SUBSTRATE

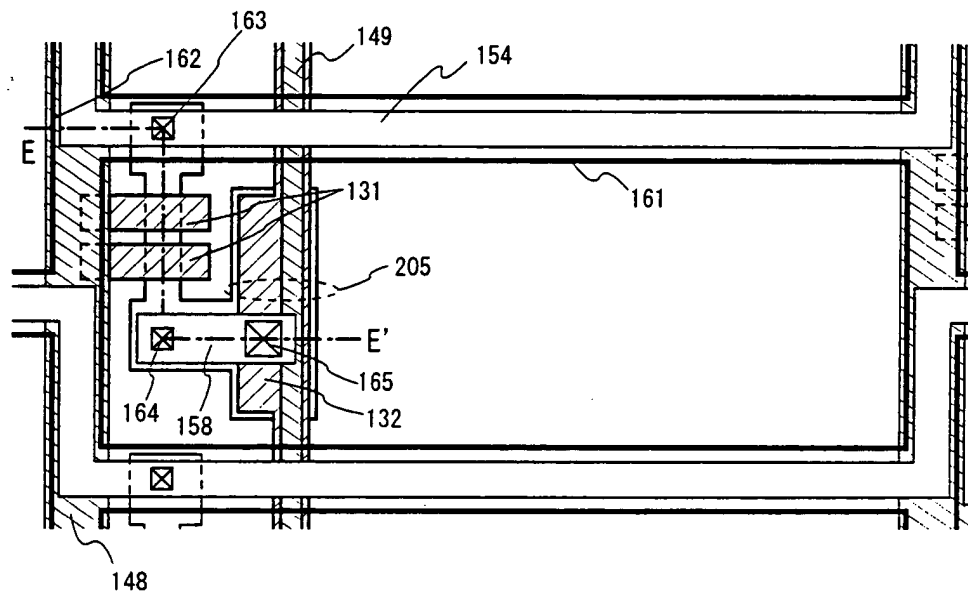


FIG. 13

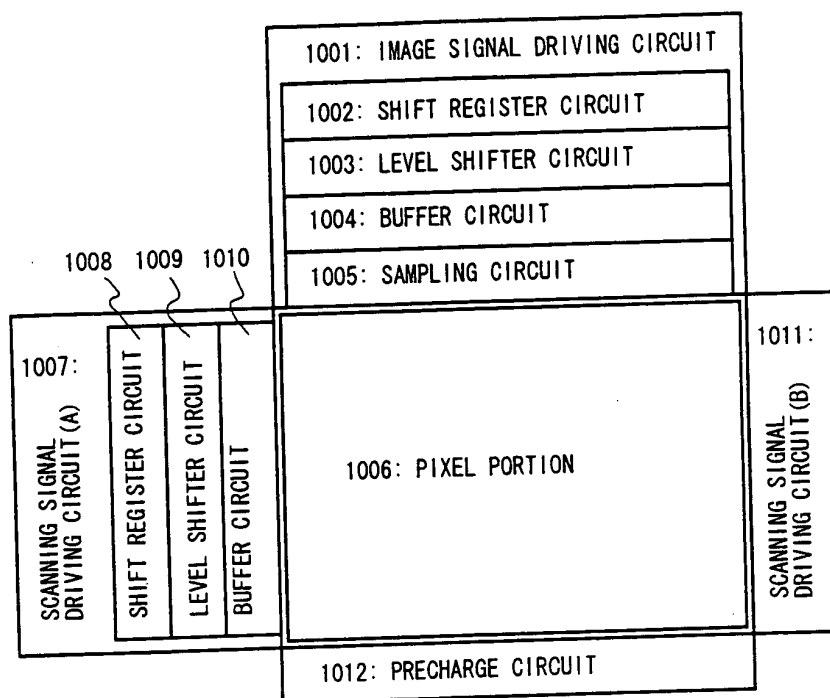


FIG. 14

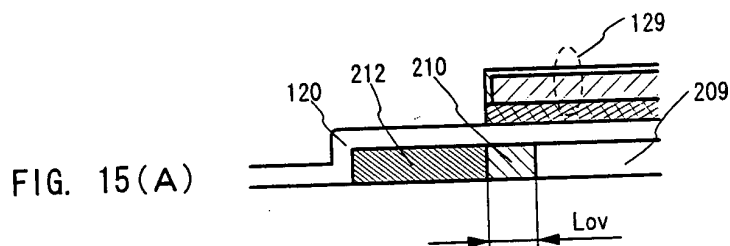


FIG. 15(A)

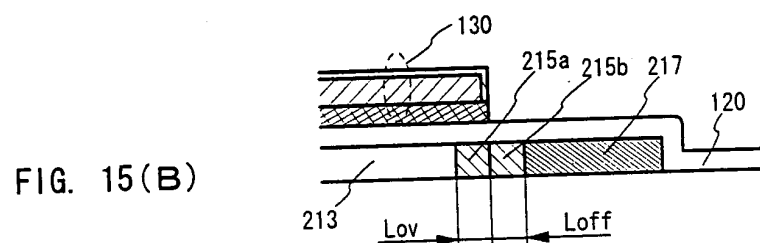


FIG. 15(B)

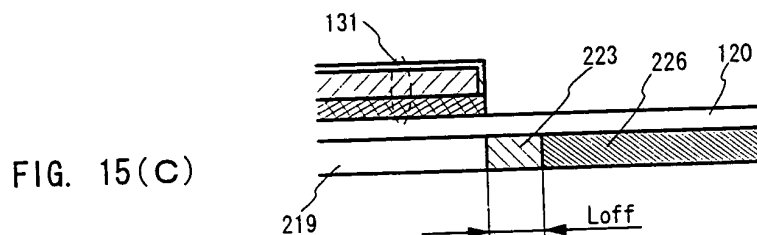


FIG. 15(C)

FIG. 16(A)

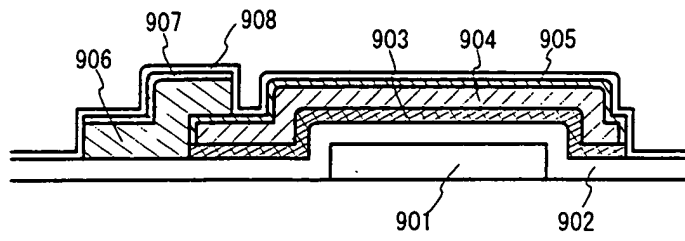


FIG. 16(B)

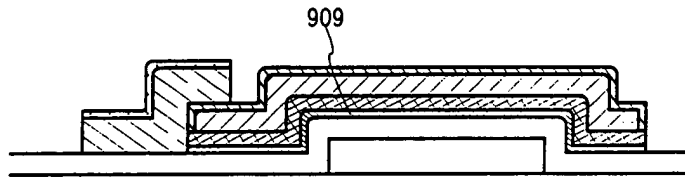
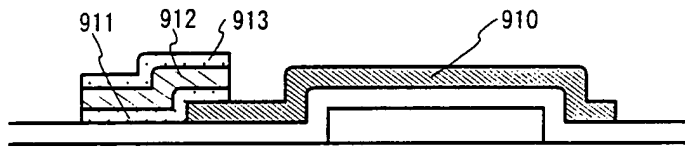


FIG. 16(C)



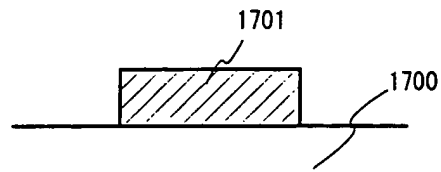


FIG. 17(A)

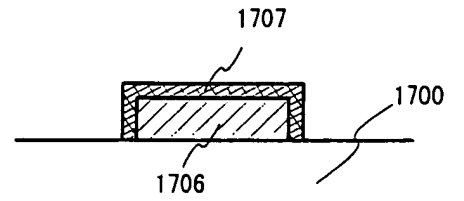


FIG. 17(D)

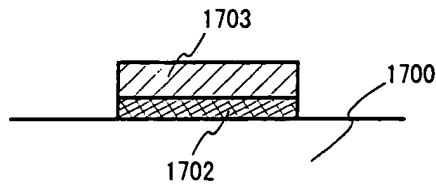


FIG. 17(B)

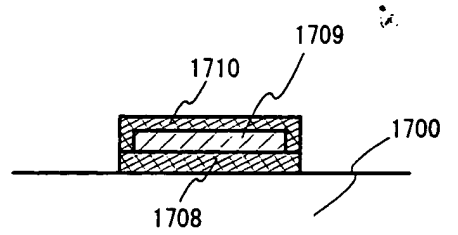


FIG. 17(E)

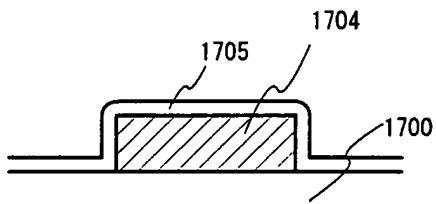


FIG. 17(C)

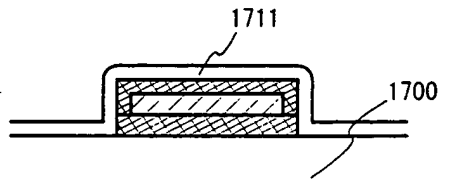


FIG. 17(F)

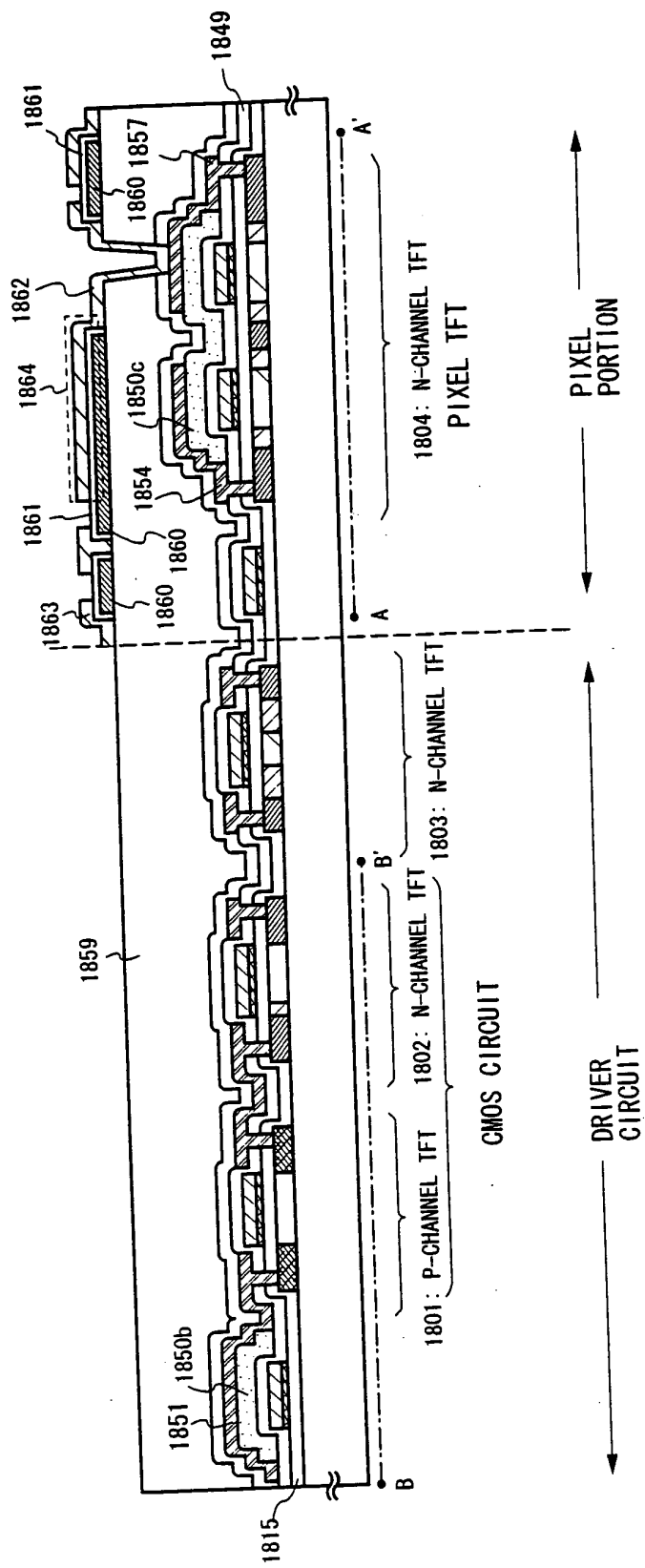


FIG. 18

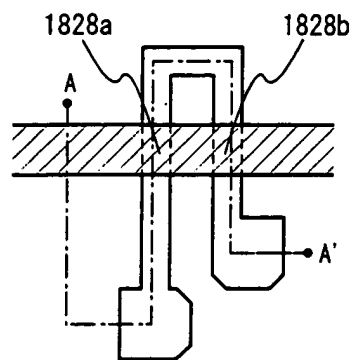


FIG. 19(A)

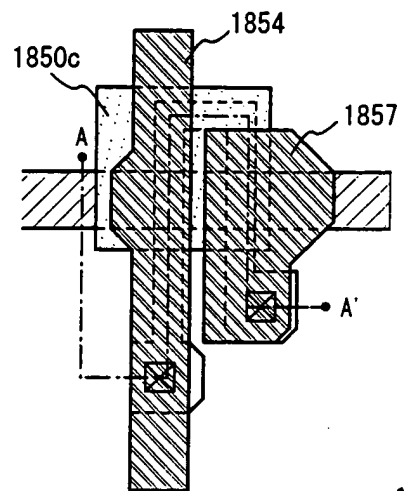


FIG. 19(B)

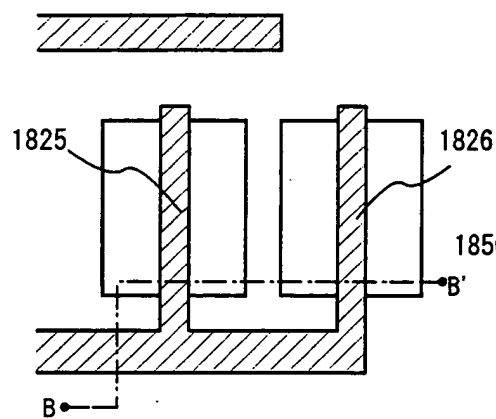


FIG. 20(A)

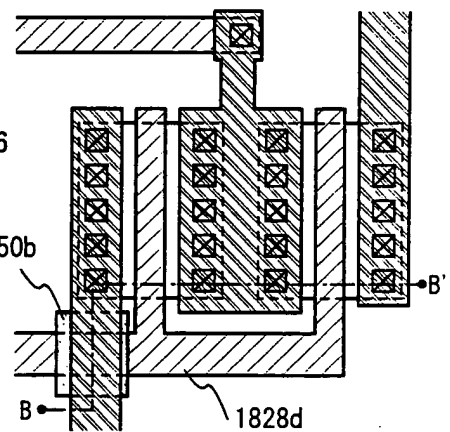


FIG. 20(B)



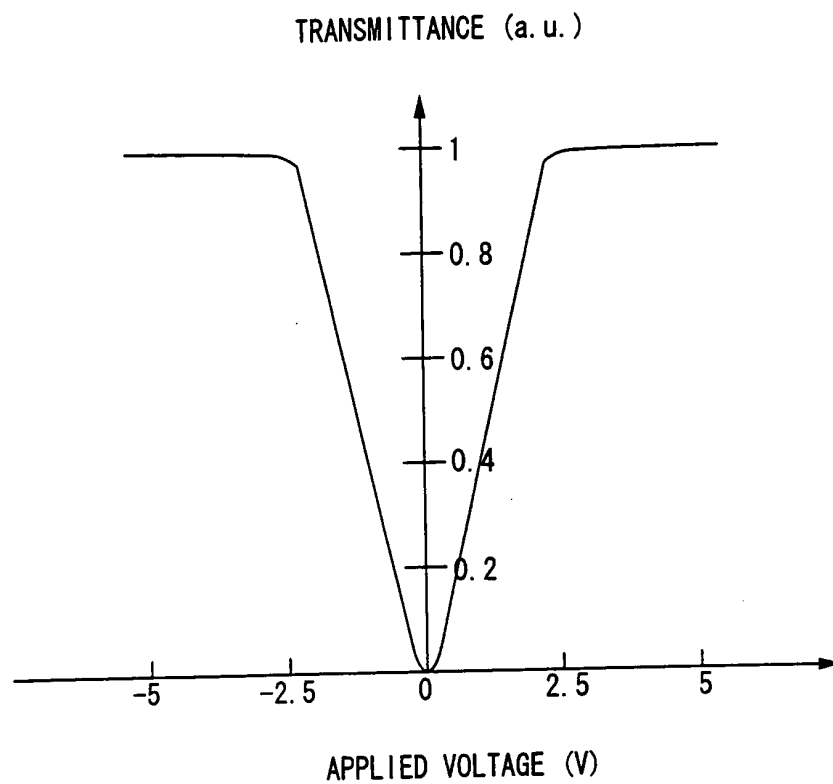
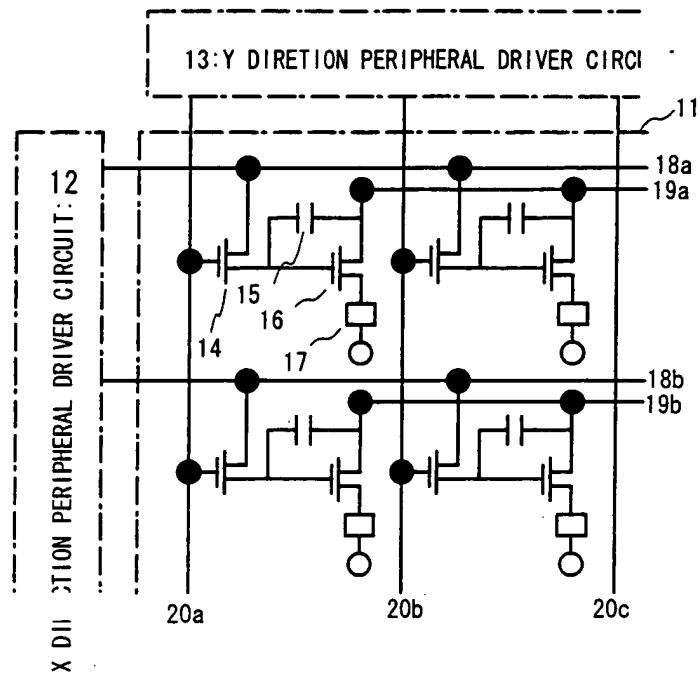


FIG. 21



- 11: PIXEL PORTION
- 12: X DIRECTION PERIPHERAL DRIVER CIRCUIT
- 13: Y DIRECTION PERIPHERAL DRIVER CIRCUIT
- 14: SWITCHING TFT
- 15: STORAGE CAPACITOR
- 16: CURRENT CONTROLLING TFT
- 17: ORGANIC EL ELEMENT
- 18A, 18B: X-DIRECTION SIGNAL LINES
- 19A, 19B: POWER SUPPLY LINES
- 20A, 20B, 20C: Y-DIRECTION SIGNAL LINES

FIG. 22

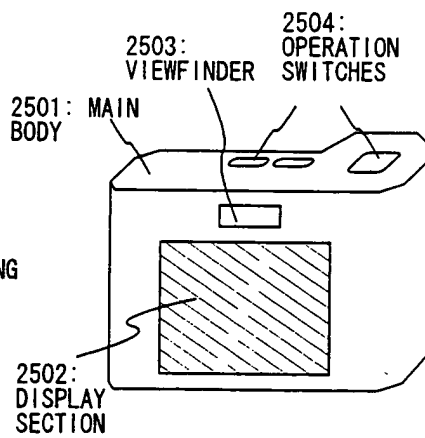
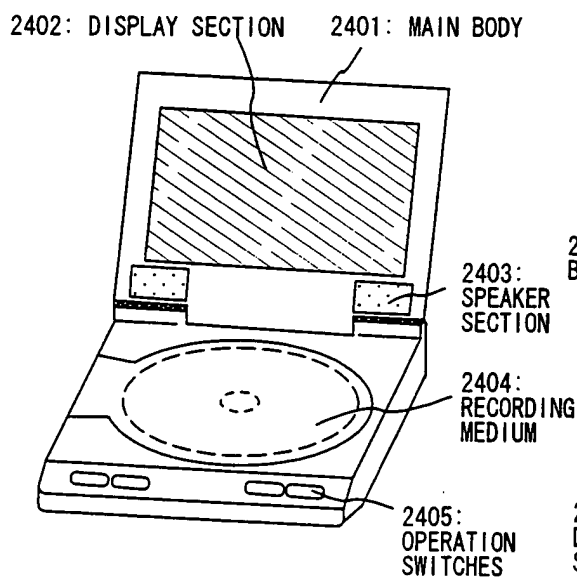
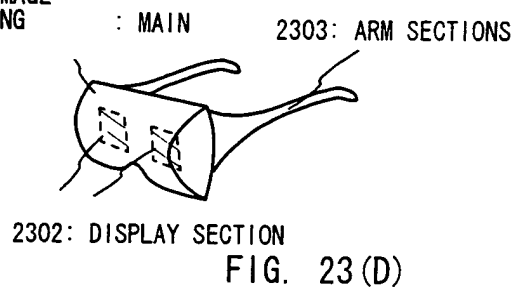
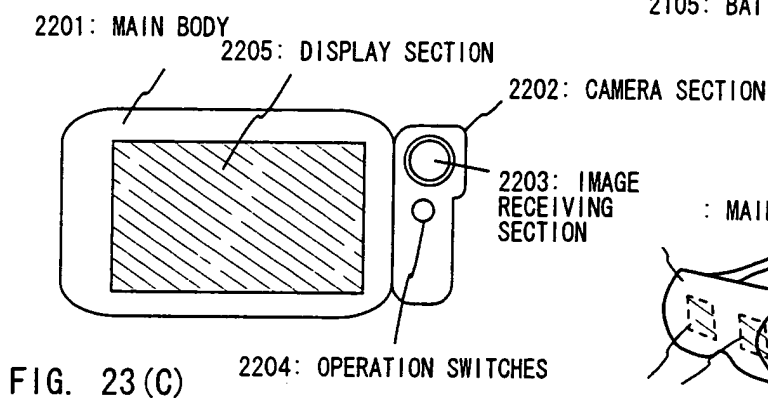
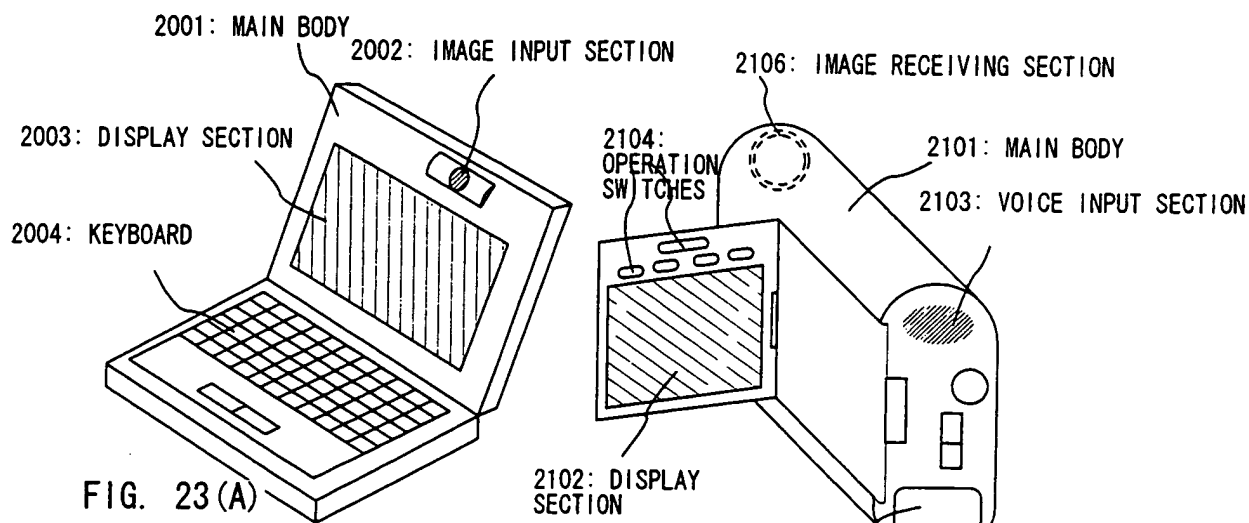


FIG. 23(E)

FIG. 23(F)

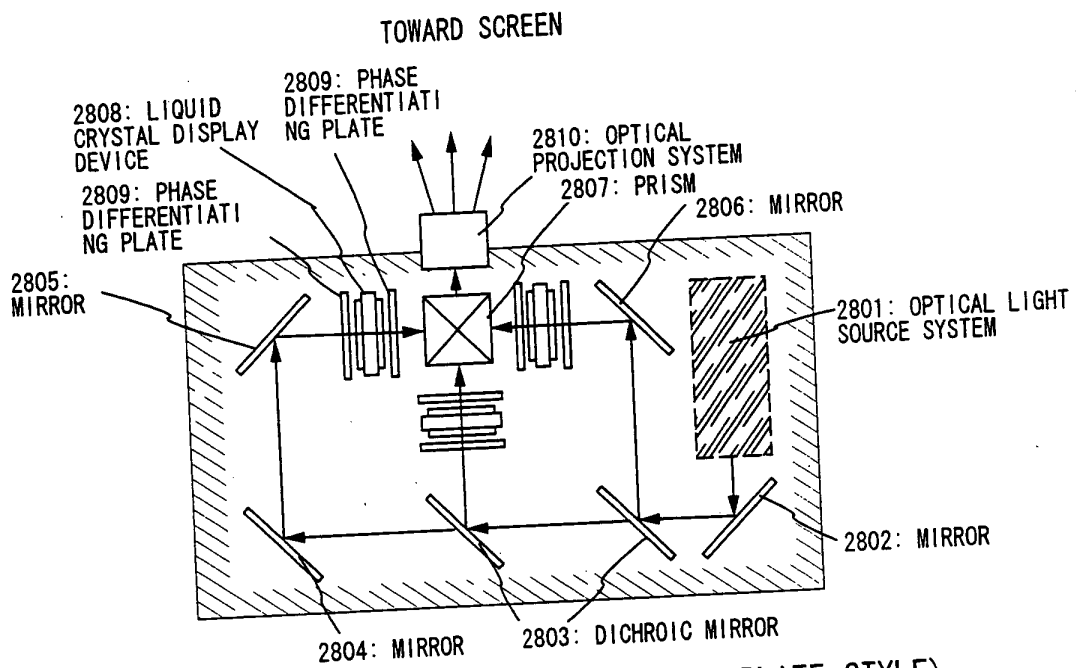
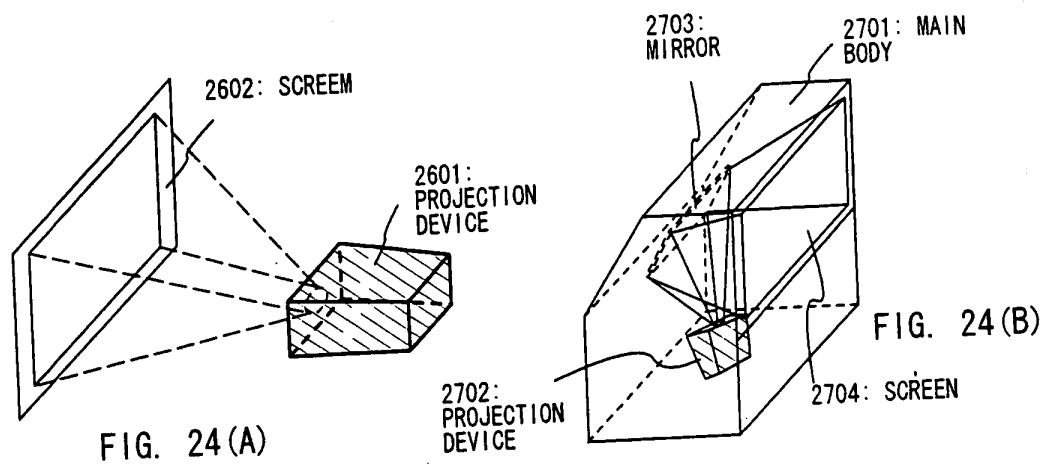


FIG. 24(C) PROJECTION DEVICE (THREE-PLATE STYLE)

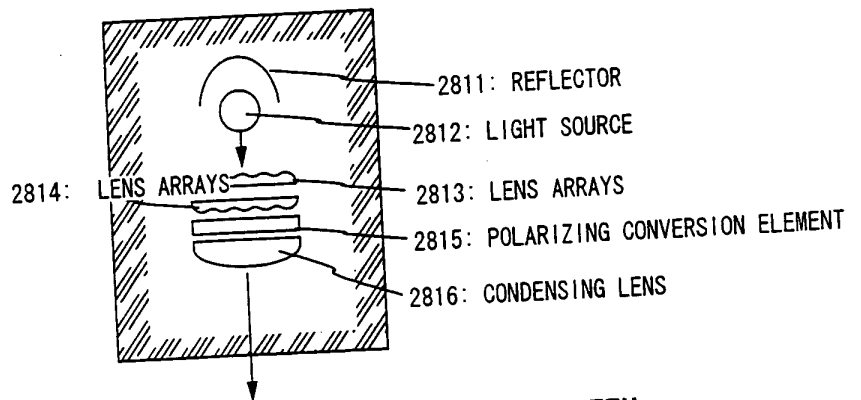


FIG. 24(D) OPTICAL LIGHT SOURCE SYSTEM

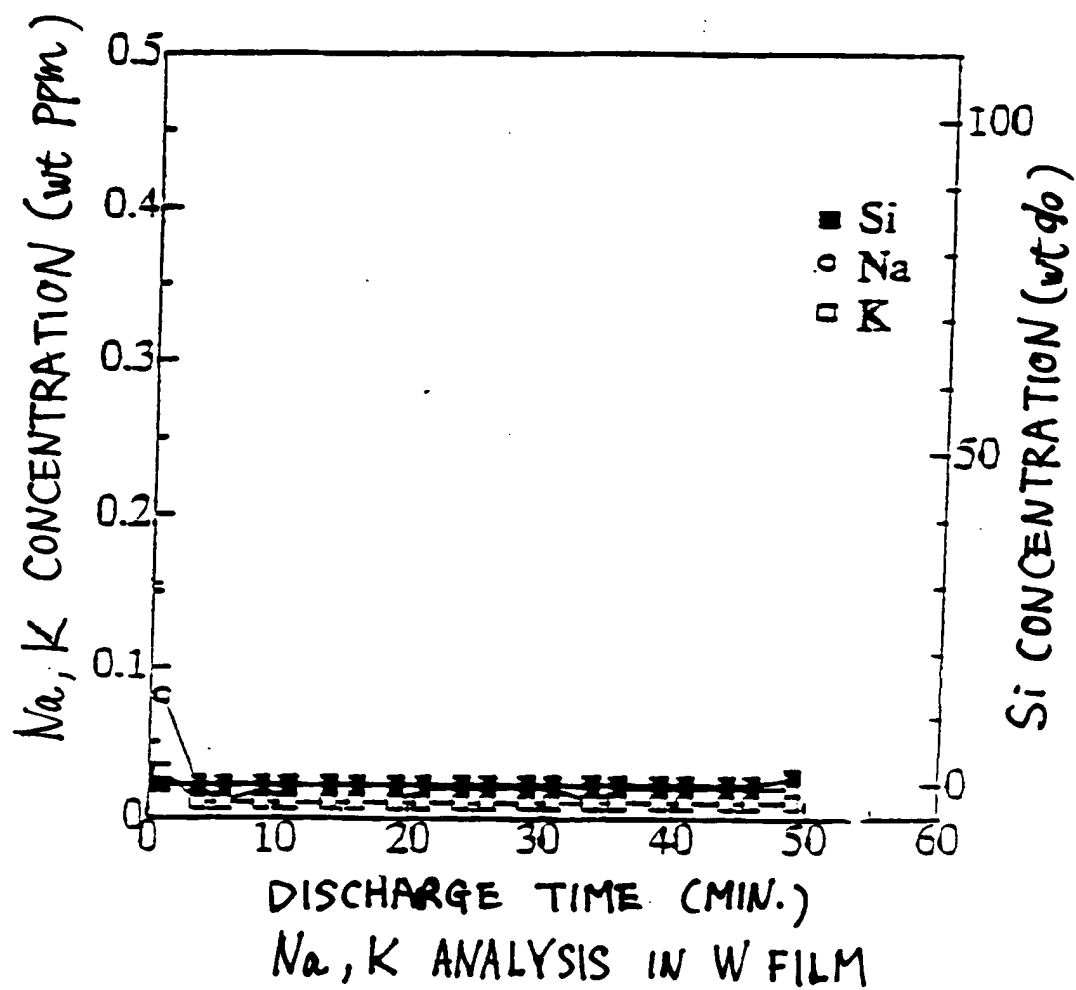
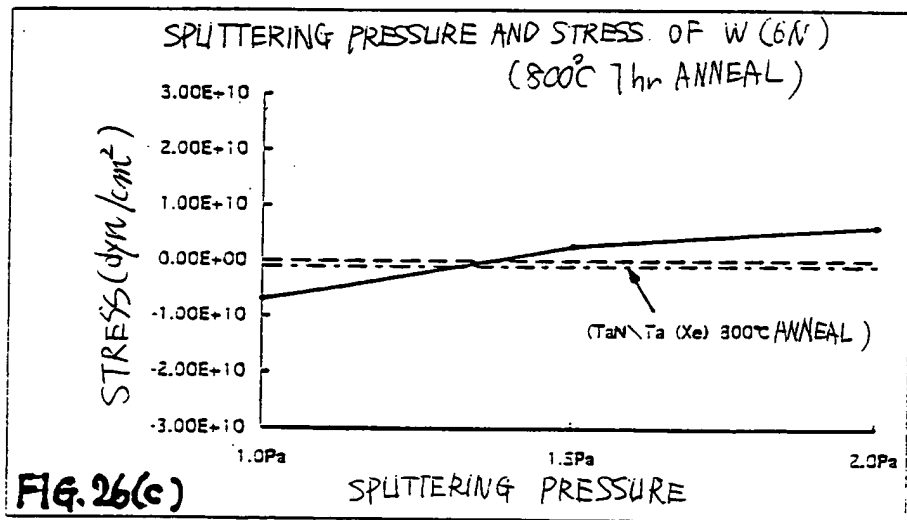
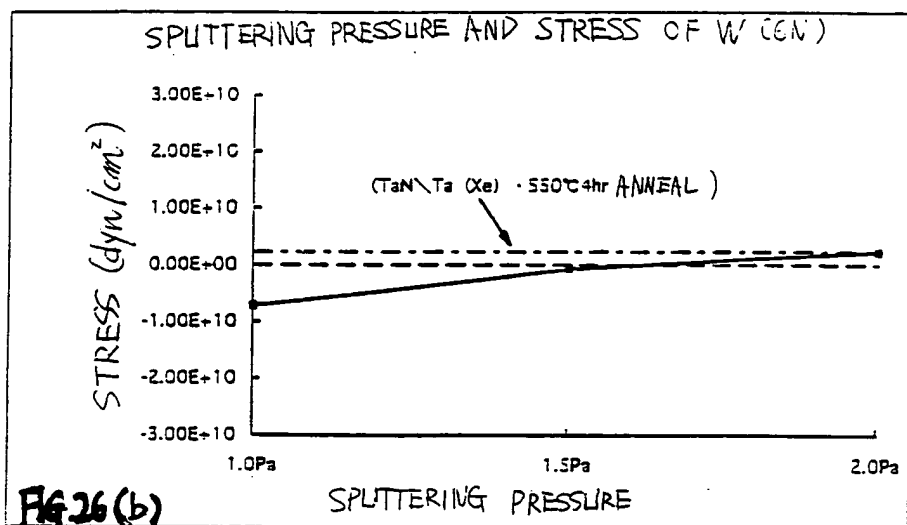
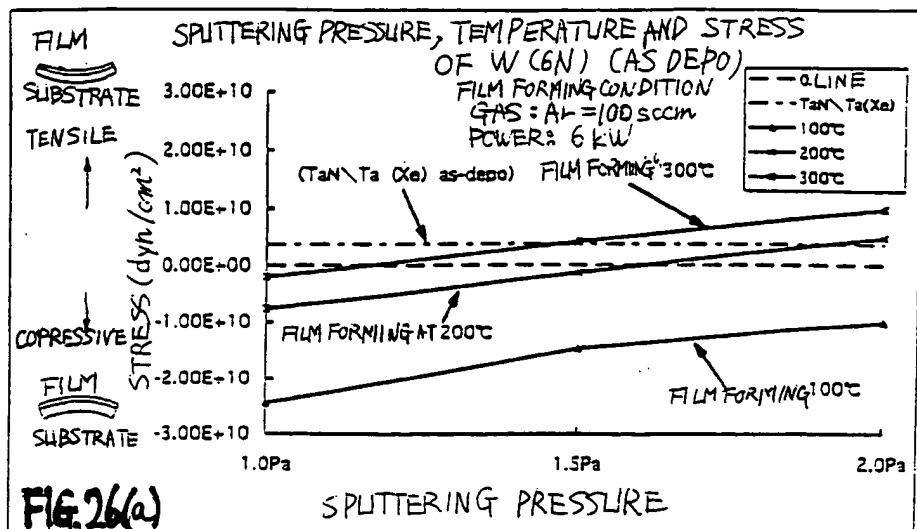
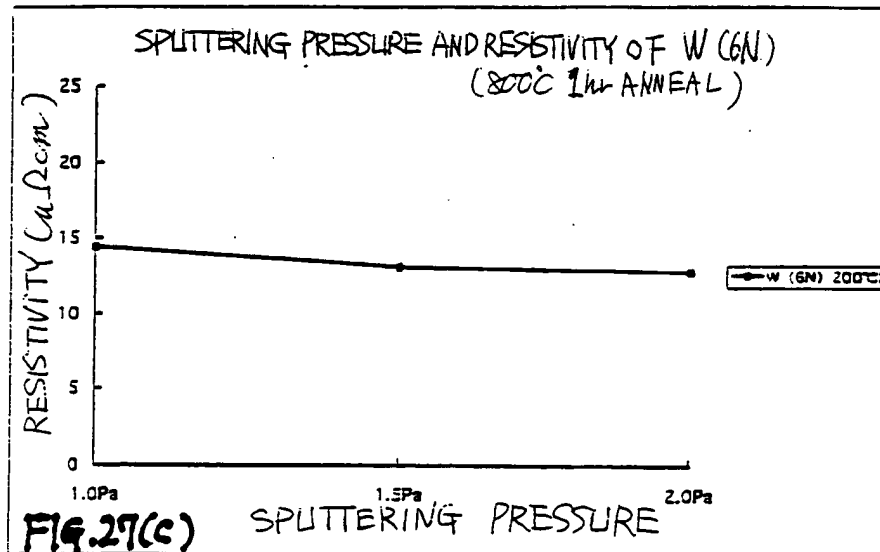
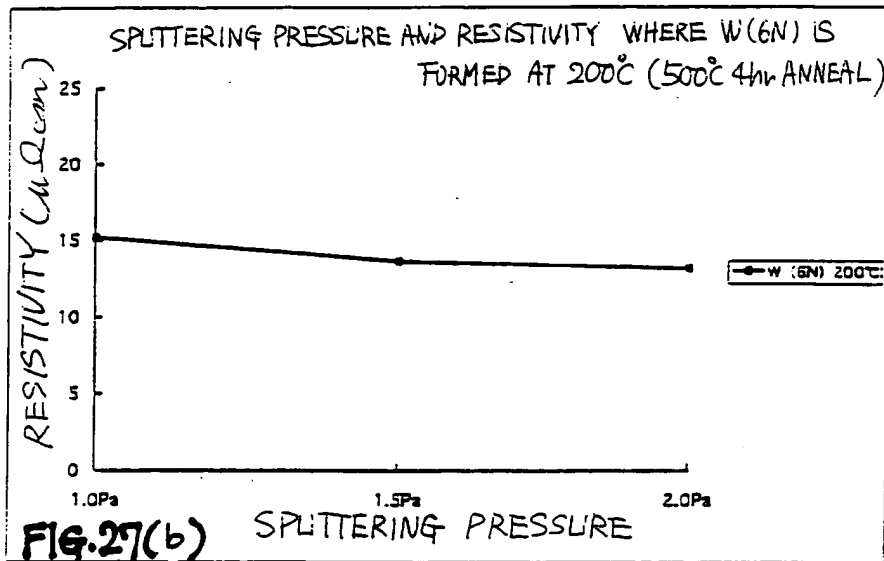
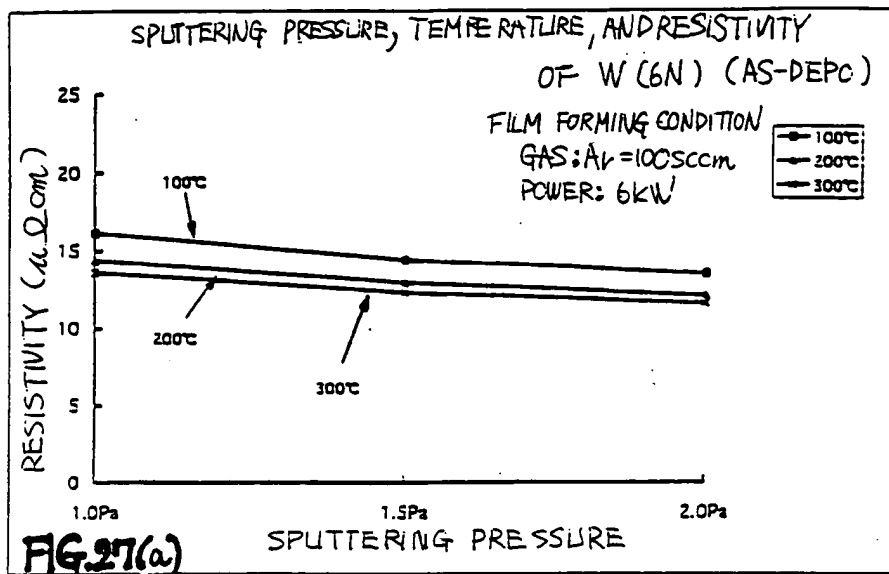


FIG.25





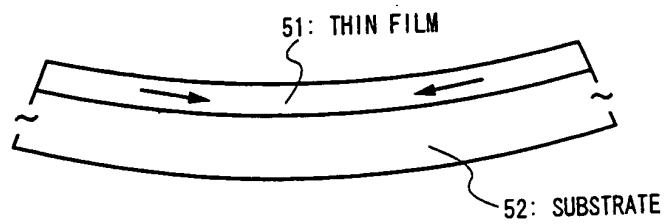


FIG. 28(A) TENSILE STRESS

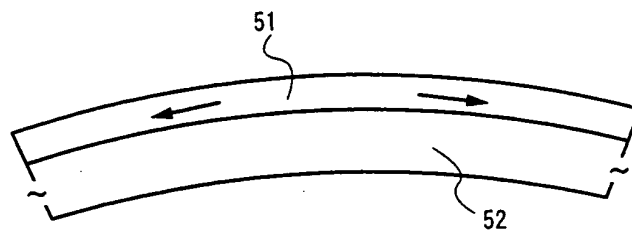


FIG. 28(B) COMPRESSIVE STRESS

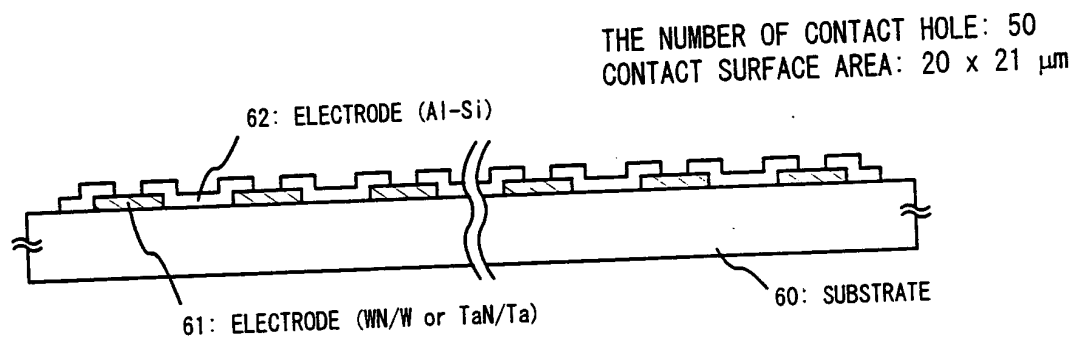
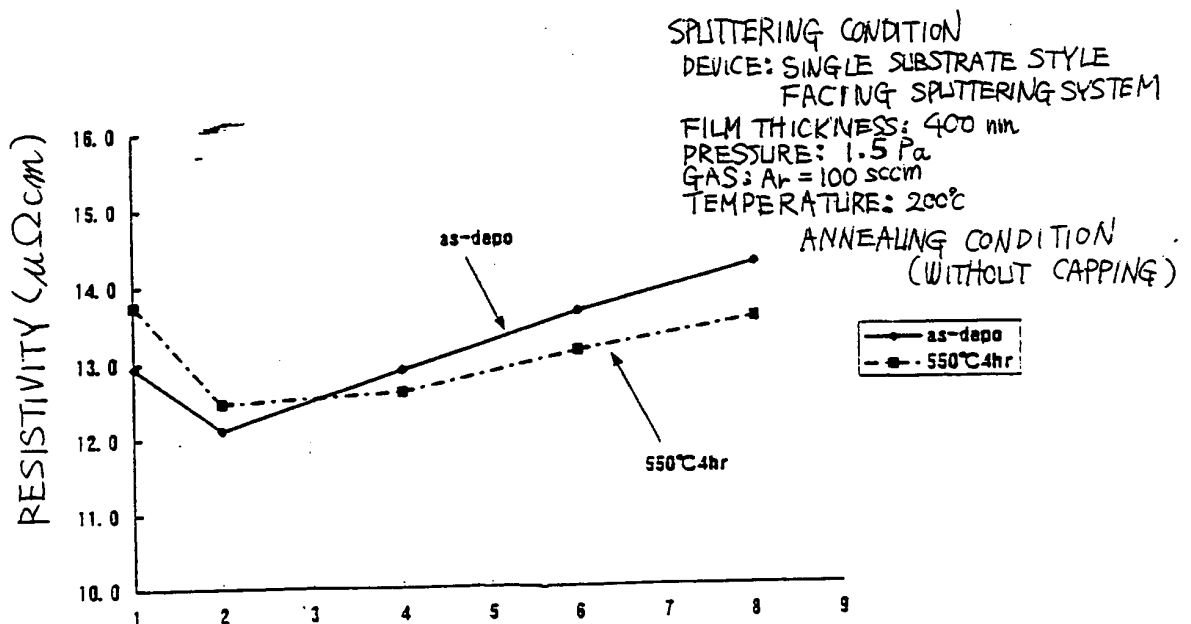
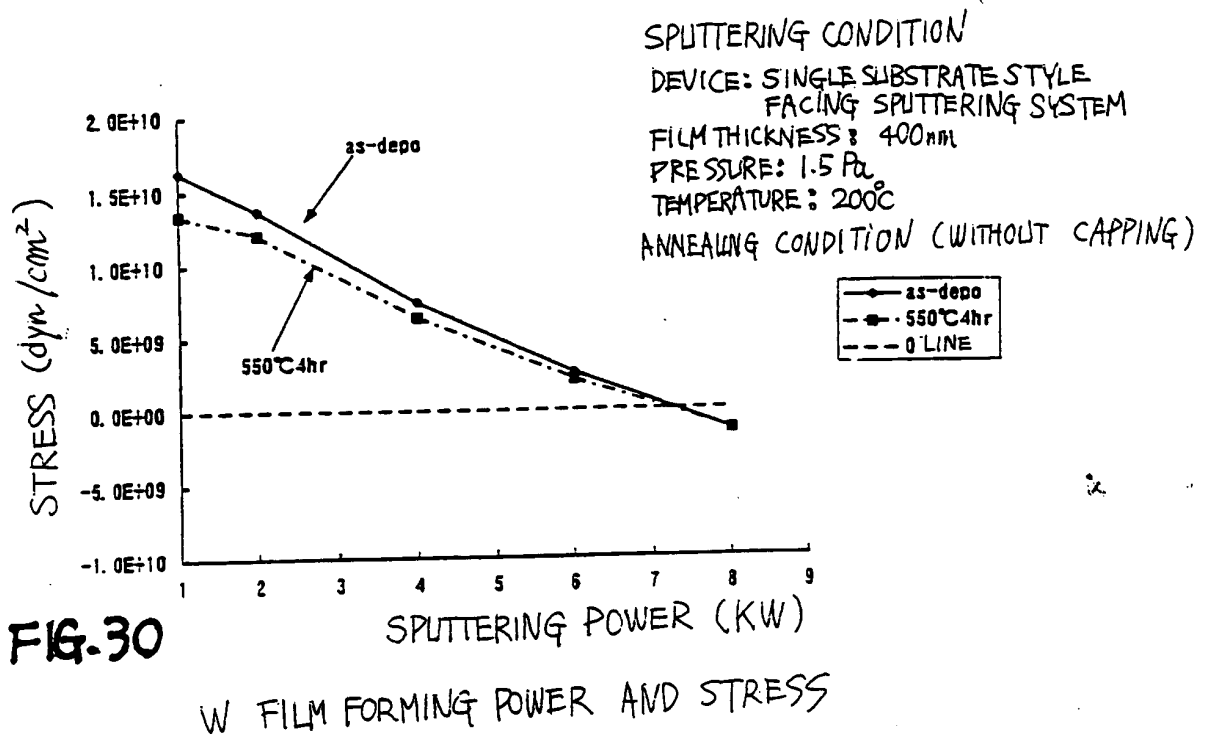


FIG. 29





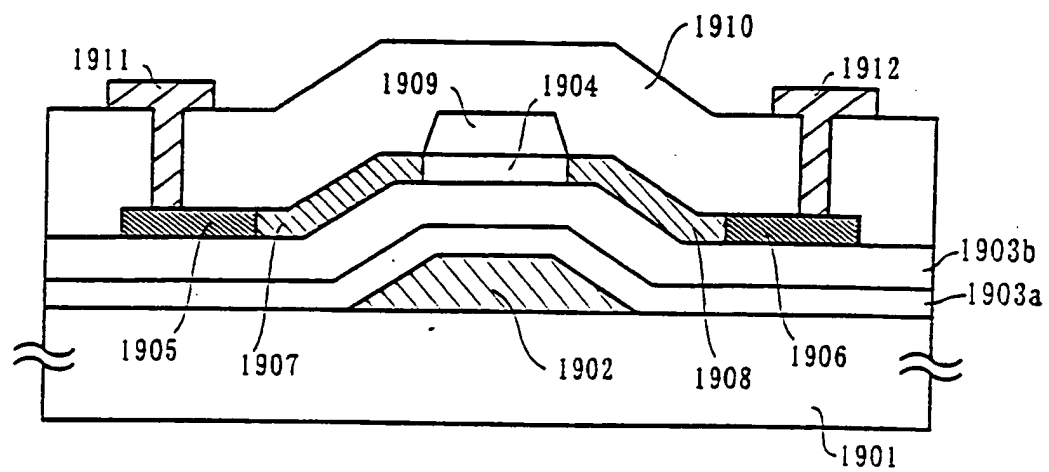


FIG. 32